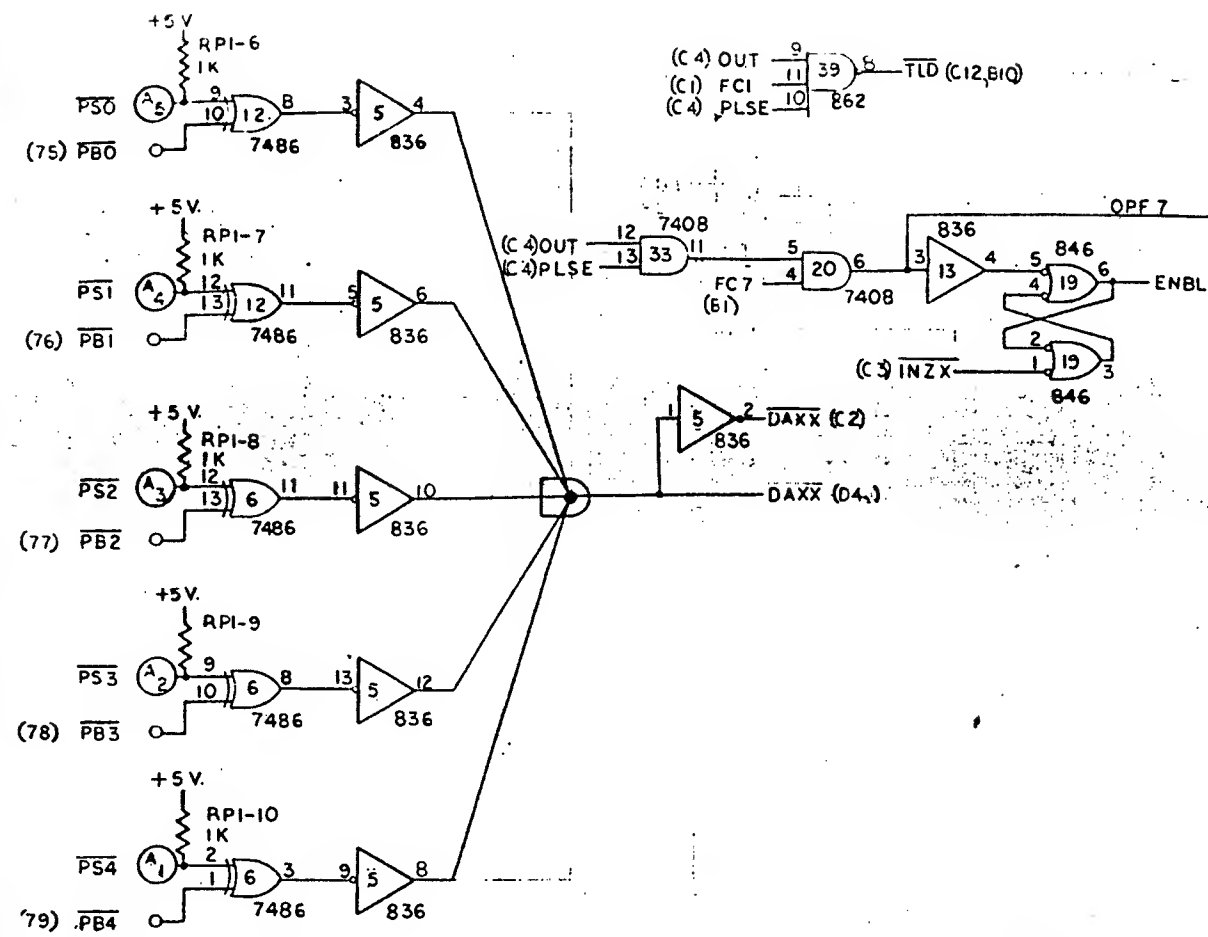
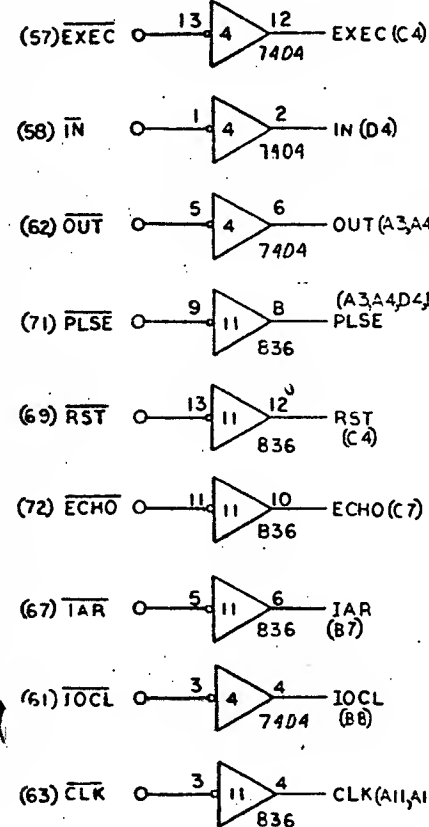


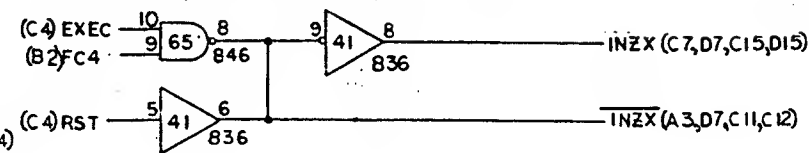
OUTPUT COMMAND DECODE



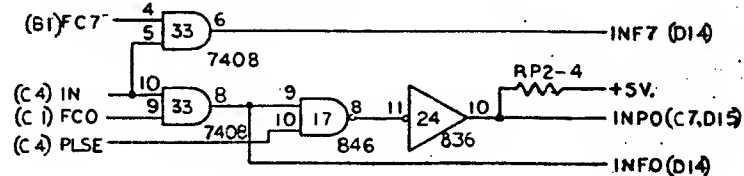
CONTROL BUS INPUTS



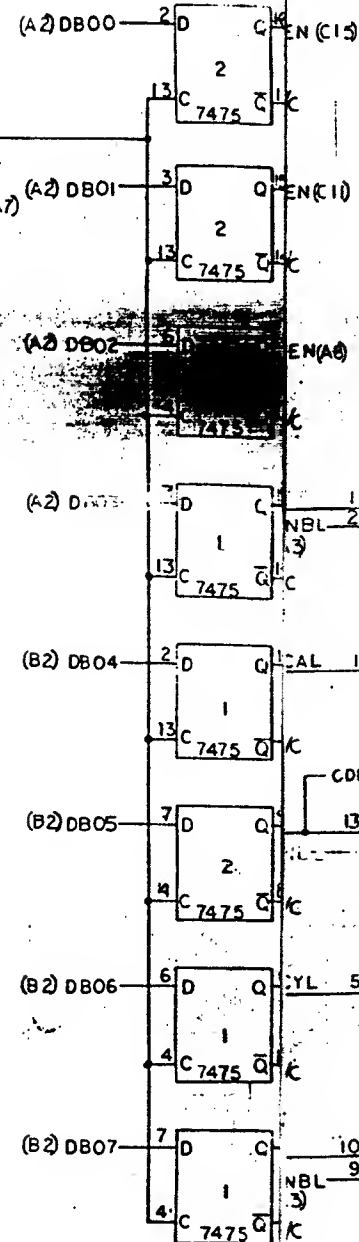
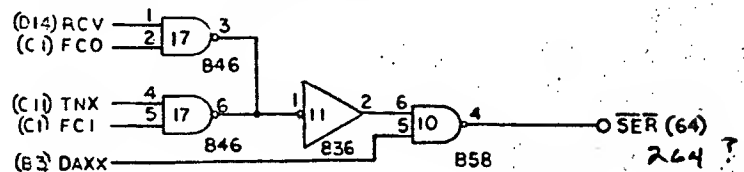
SELECT COMMAND DECODER



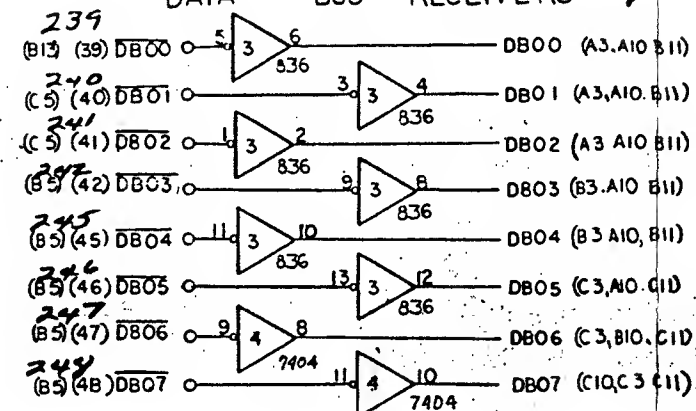
INPUT COMMAND DECODER



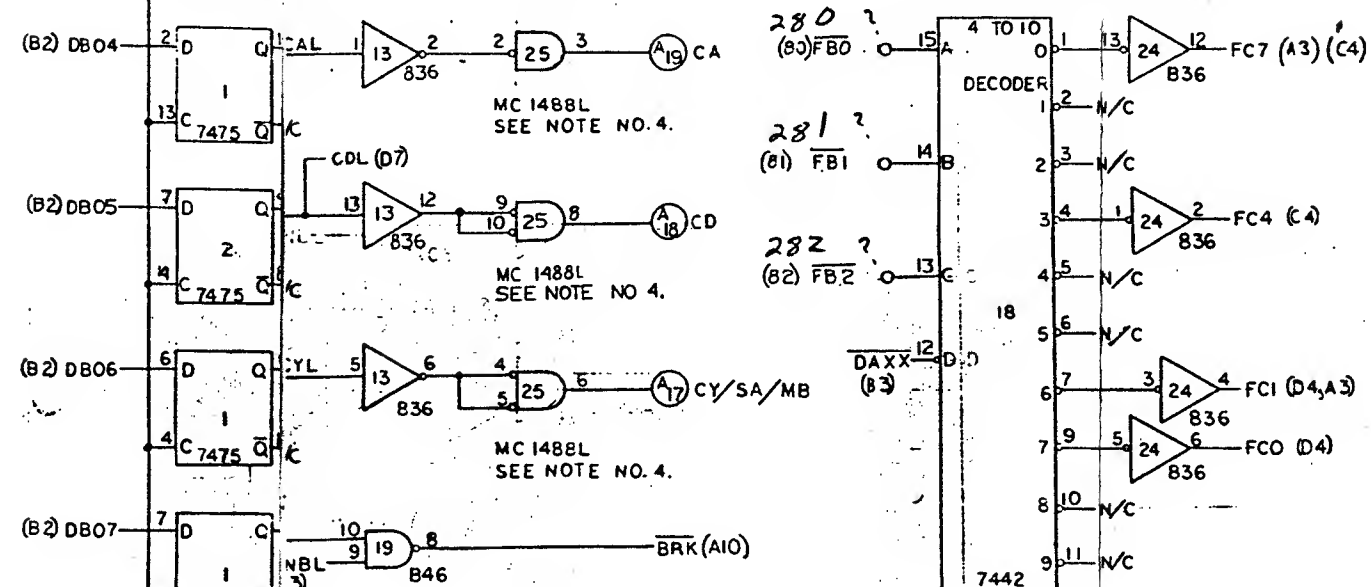
SENSE ENCODER



DATA BUS RECEIVERS



FUNCTION DECODER




REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A0	INITIAL RELEASE		
A1	INCORP EN 53227-XX-A1		
A2	INCORP EN 53227-XY-A2		
A3	INCORP EN 53227-VV-A3		
A4	INCORP EN 53227-XY-A4	1-6-73	Revised

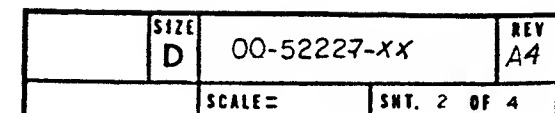
4. VCC & GRD. INJECTIONS AS FOLLOWS: +15 PIN 14, -15 PIN 1,
GRD PIN 7. MC1488L ONLY.
3. SEE DWG. 53227-0X FOR ASSY. DWG.
2. REF DESIG. IONS NOT USED C15, C16.
1. ALL RESIS S ARE 1/4 WATT, 5%.

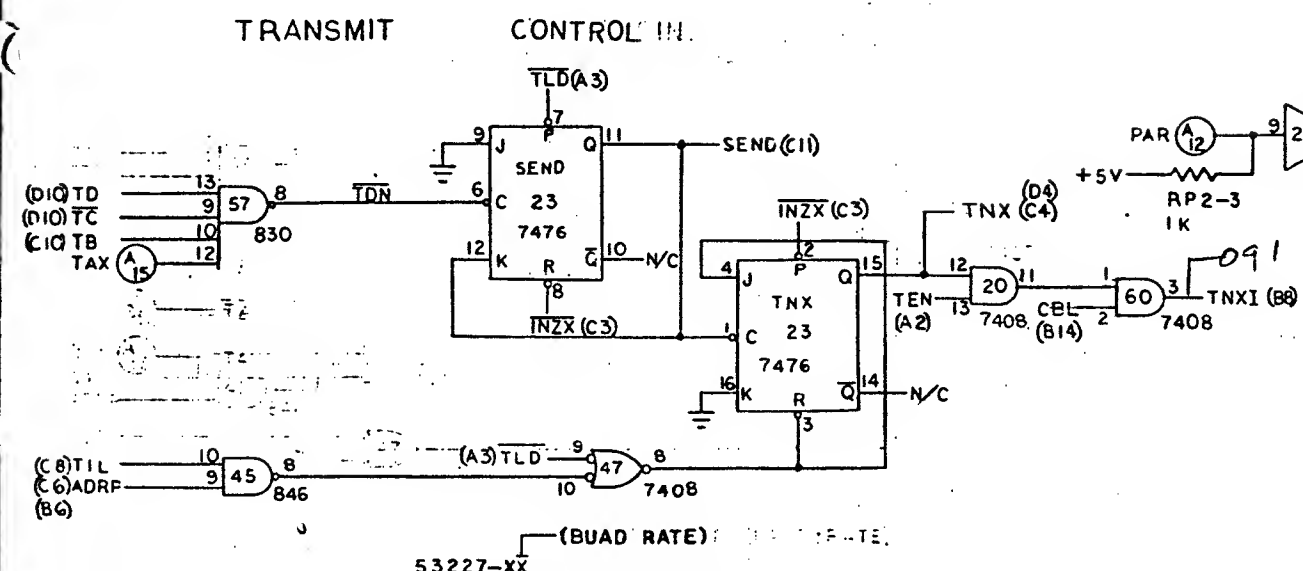
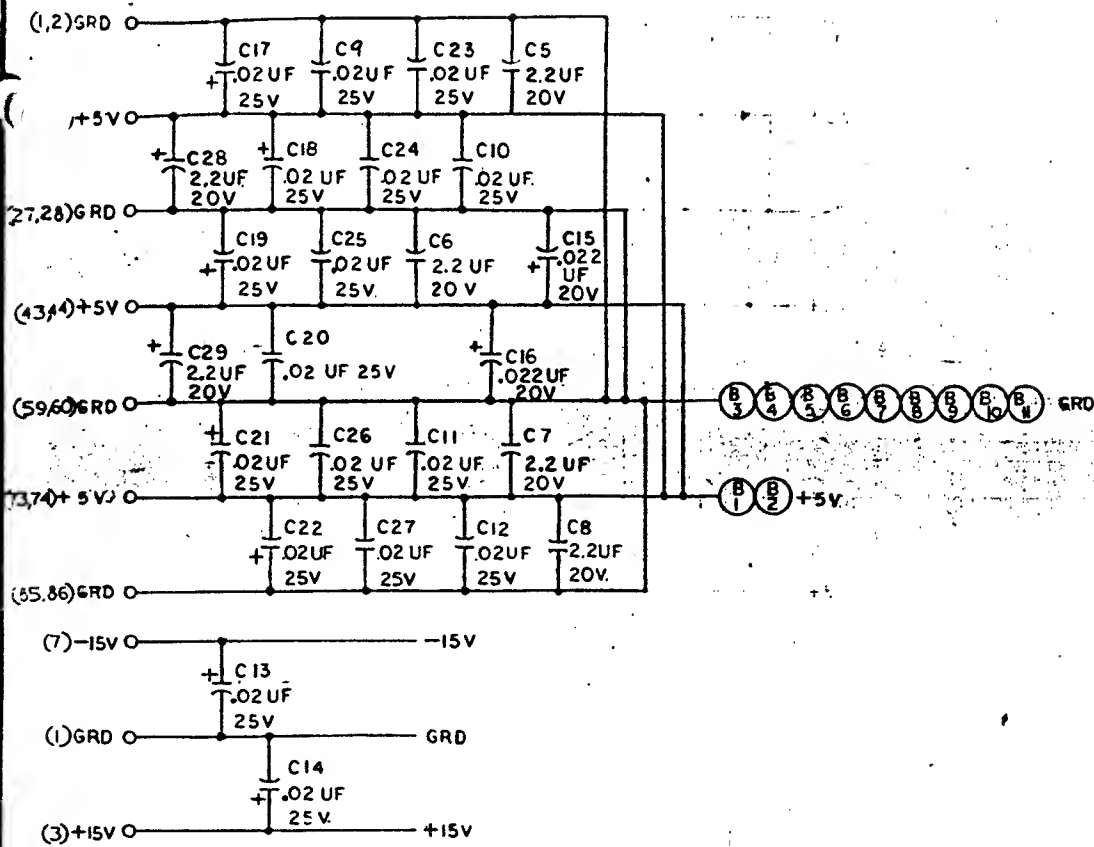
NOTES: UNLESS OTHERWISE SPECIFIED:

DASH NO.	NEXT	ASSY	QTY REQD	OSG	
				ENGR.	
				PROJ	
				REL	
				TOLERANCES	
				.X = $\pm .1$	
				.XX = $\pm .03$	
				.XXX = $\pm .010$	
				ALL HOLE DIAMETER ARE PLATING	

Q.	DESCRIPTION	MAT'L. VENDOR
	LIST OF MATERIAL	
	COMPUTER AUTOMATION INC. 	
	888 WEST SIXTEENTH STREET, BEVERLY BEACH, CALIFORNIA 92660	
	LOGIC DIAGRAM ASYNCHRONOUS DATA SET CONTROLLER, ALPHA	
	SIZE D	REV 84
	00-52227-8X	
S	SCALE =	SHT. 1 OF 4

ANSWER

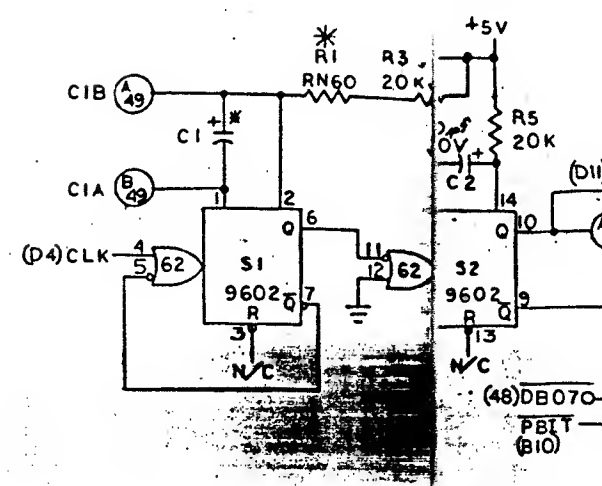




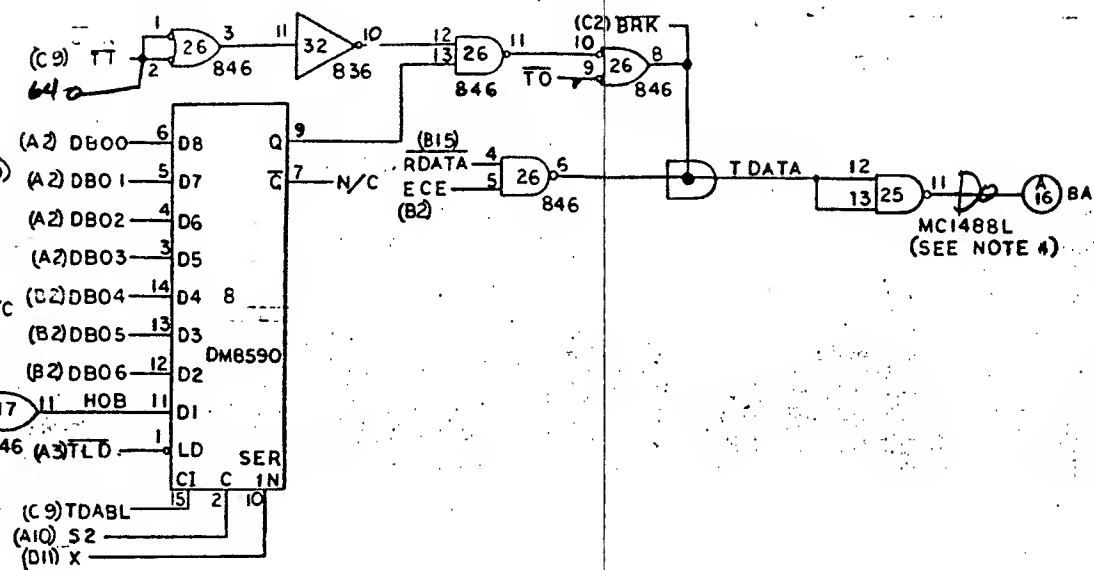
DIGIT NO.	BAUD RATE	VALUE C1	VALUE C3	VALUE R1	VALUE R2
-11	110	1.5 UF	.68 UF	14.3K	14.3K
-12	150	1.5 UF	.68 UF	14.3K	14.3K
-13	300	1.5 UF	.68 UF	4.99K	4.99K
-14	600	.33 UF	.15 UF	14.3K	14.3K
-15	1200	.15 UF	.082 UF	4.99K	4.99K
-16	1800	.15 UF	.082 UF	4.99K	4.99K
-17	2400	.15 UF	.082 UF	4.99K	4.99K
-18	4800	.039 UF	.039 UF	4.99K	4.99K
-19	9600	.015 UF	.015 UF	4.99K	4.99K

+5V
RP2-2
1K
X (A13, B10, D11, B14)

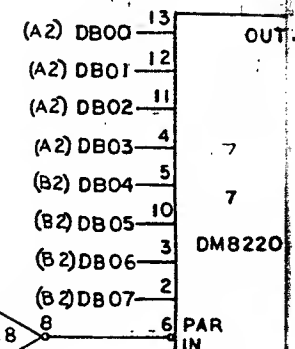
TRANSMIT SHIFT GENERATOR



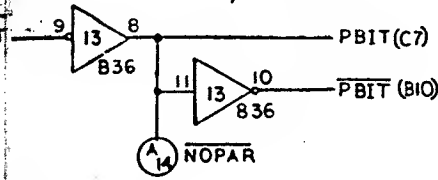
TRANSMIT DATA REGISTER LOGIC



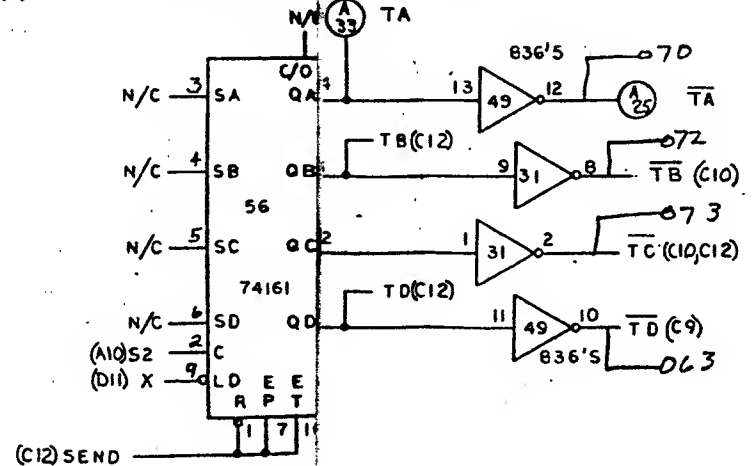
PARITY



GENERATOR/CHECKER

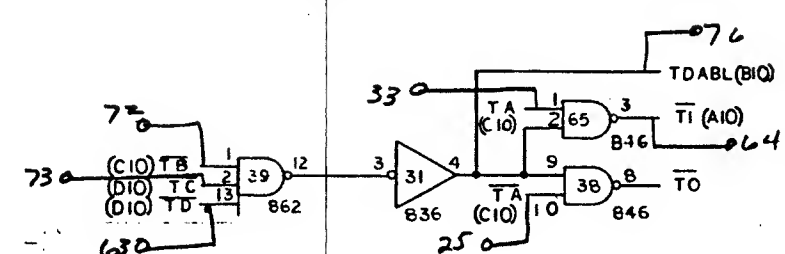


TRANSMIT SHIFT COUNTER

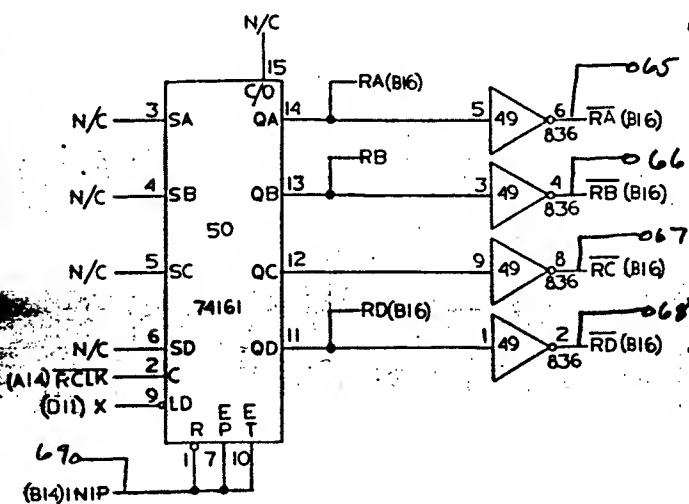


* TEST
SEE TABULATION BLOCK (THIS SHIT)

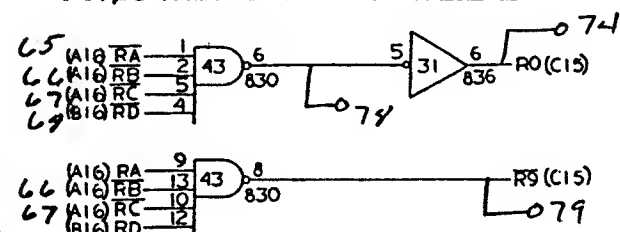
P/O TRANSMIT CONTROL



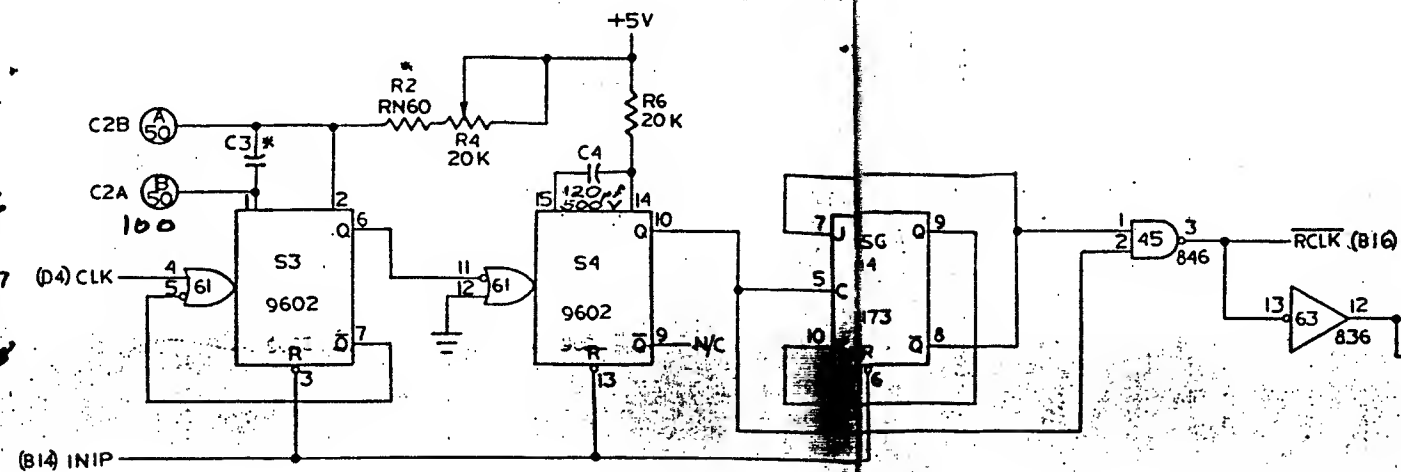
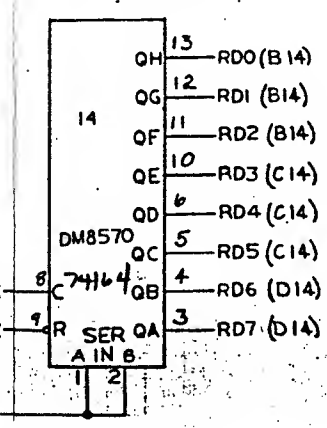
RECEIVE SHIFT COUNTER



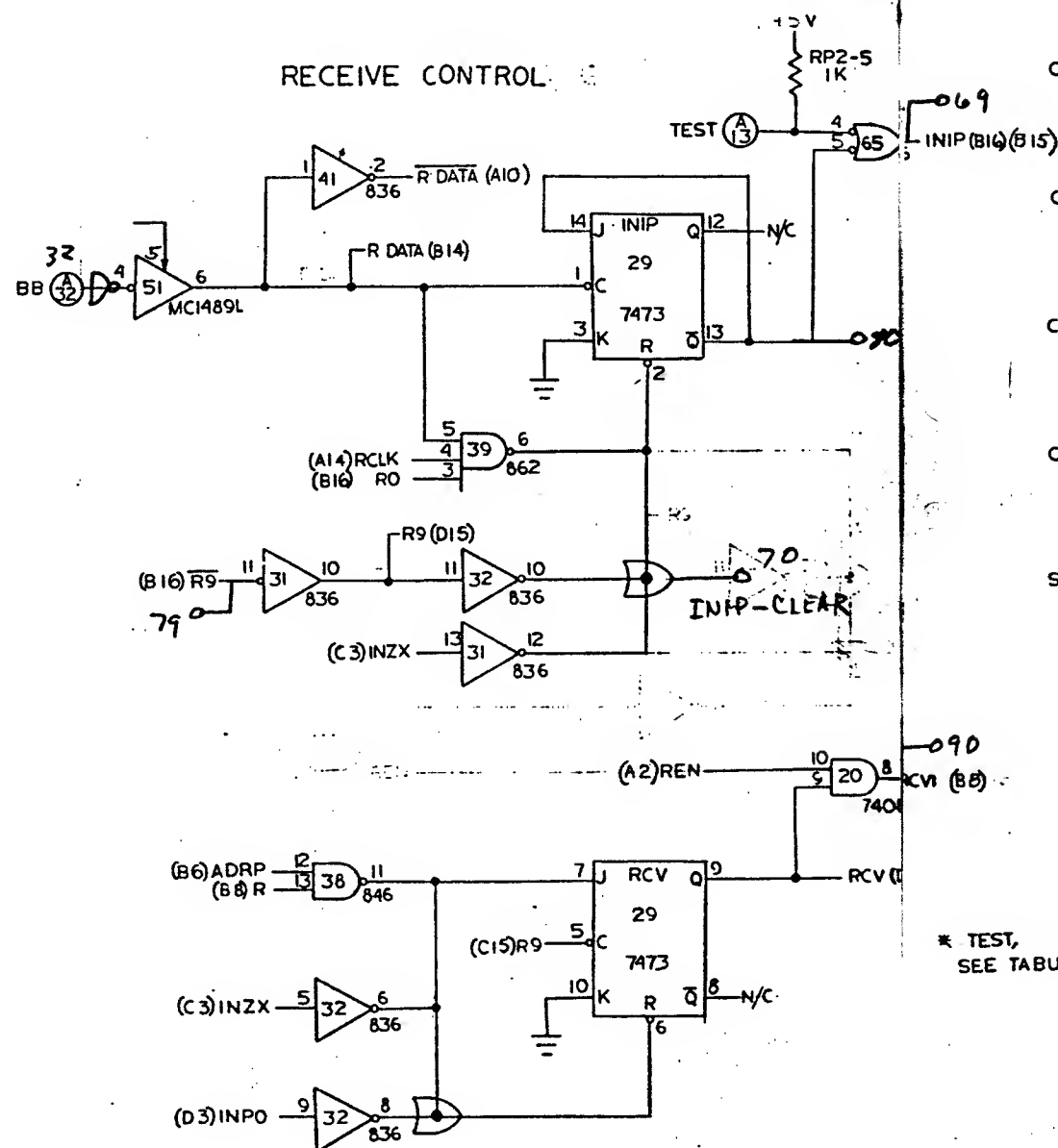
P/O RECEIVE CONTROL



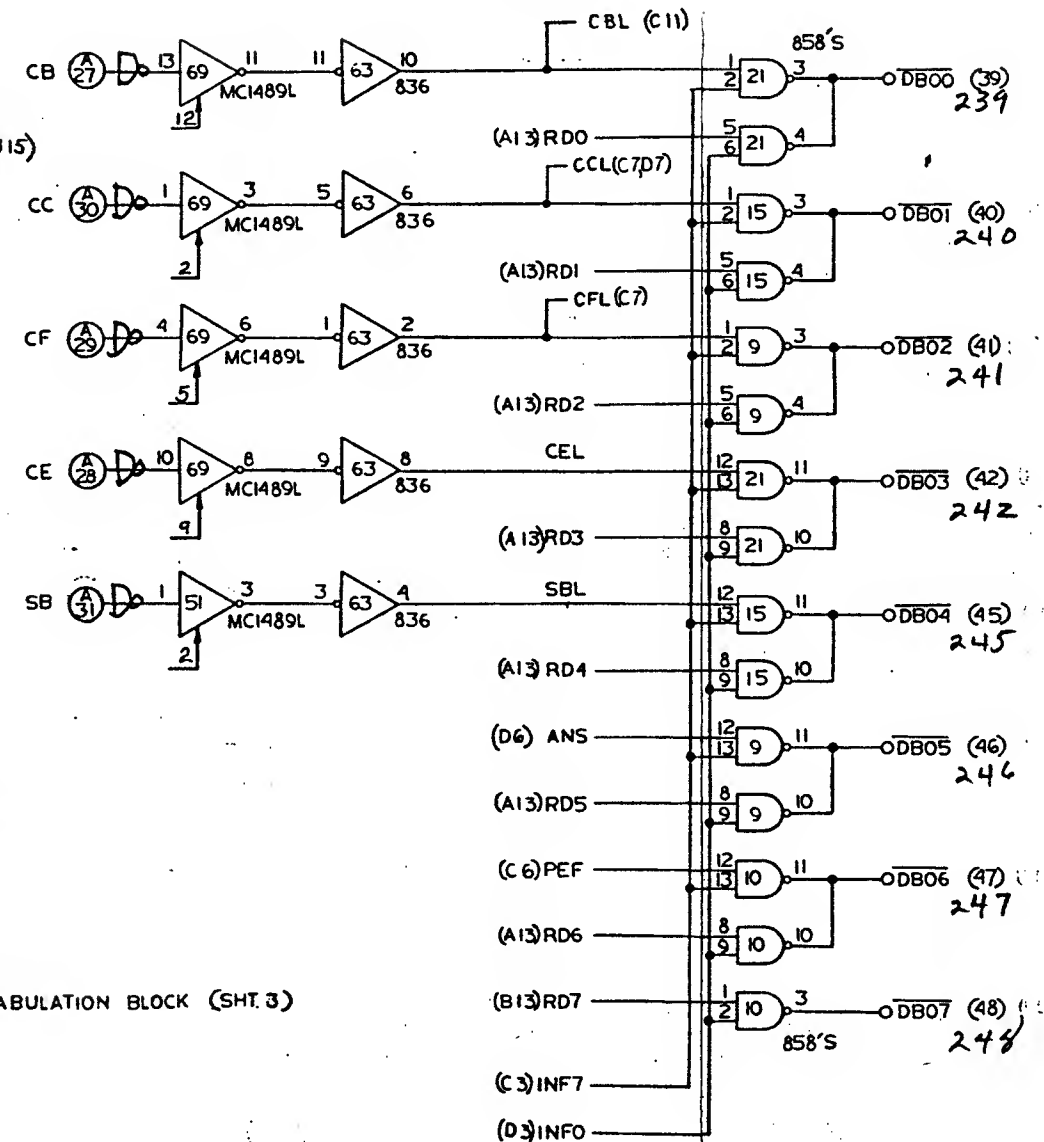
RECEIVE SHIFT GENERATOR

RECEIVE
DATA
REGISTER.

RECEIVE CONTROL.



DATA BUS DRIVERS



* TEST,
SEE TABULATION BLOCK (SHT.3)